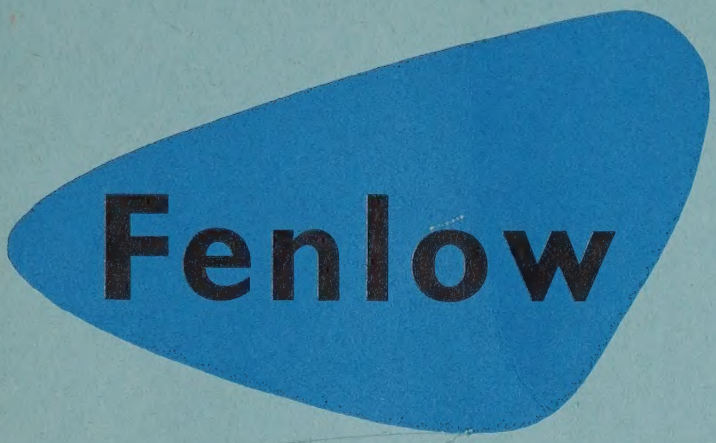
BOARD OF TRADE
TELS R2 (c)
WOBURN PLACE



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Fenlow Electronics Ltd
SPRINGFIELD LANE
WEYBRIDGE · SURREY

MP MASTER
MA23402

OPERATIONAL AMPLIFIER

TYPE A7

INSTRUCTION MANUAL

Fenlow Electronics Ltd.
Woodbridge, Surrey.

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1. Specification

Output: Linear operation to $\pm$ 100V at 50mA. Full output to 5Kc/s. Fast recovery limiting. Visual limit and overload indication.

D.C. Gain: Greater than 3×10^7.

Gain-bandwidth product: 10 megacycles. (Gain greater than 10,000 at 1Kc/s).

Input impedance: 100Kohms D.C. to 10c/s.
10Kohms above 10c/s.

Noise: Less than 50 microvolts peak-to-peak, 10 microvolts r.m.s.

Unity integrator drift: (1M, 1uF) Less than 2mV/min.

Power requirements: $\pm$ 150V at 40mA standing current rising to 90mA when supplying maximum output.

Dimensions: The amplifier occupies 1.2 inches width in a standard 19" x 7" rack mounting modular frame (Imhof MCF4D10) and is 10 inches deep. 14 amplifiers fit one frame.

THE A7 OPERATIONAL AMPLIFIER

2. General

The A7 is a high voltage operational amplifier designed for use in analogue and hybrid computer applications. It can also be used in a wide range of instrumentation, typical examples of which are given in the Application Notes on Fenlow D.C. Amplifiers and in servo applications. It may, for instance, be used to drive split field D.C. servo motors directly.

The normal method of connecting the amplifier is shown in Fig. 1.

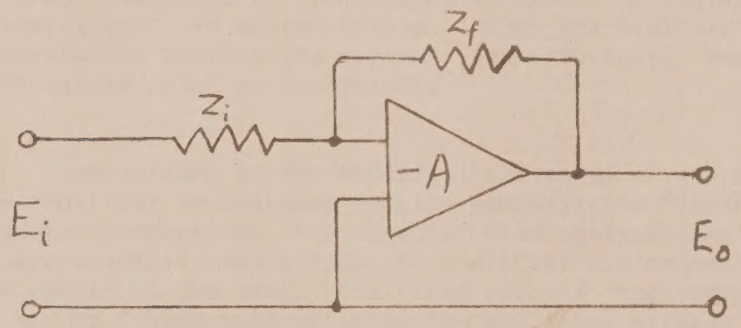

Fig. 1

The amplifier behaves as a self balancing device. Feedback current through Z_f cancels the input current through Z_i to give a null point or "virtual earth" at the summing junction which is the input terminal of the amplifier. Errors are minimized by providing a high open loop gain so that the demanded input signal is small. Spurious signals, i.e. drift and noise components at the input terminal are eliminated as far as possible. Two basic assumptions can then be made. These are that the current flowing into the amplifier from the summing junction and the voltage between summing and junction and common are both zero. The relation between E_o and E_i is then given by

$$\frac{E_o}{E_i} = \frac{Z_f}{Z_i}$$

If Z_i and Z_f are both resistors the amplifier gives a voltage gain = R_f/R_i. In another commonly used configuration Z_i is a capacitor. The unit then behaves as an integrator with E_o given by $\frac{1}{CR}\int E_i dt + k$ where k is the initial voltage across the capacitor.

The A7 requires power supplies to give plus and minus 150V stabilized to about .1% for best performance. Each amplifier requires 40mA per line standing current rising to a maximum of 90mA on full load. Two special power units are available, the PU5 and PU7. Two PU5's will drive a full rack of fourteen A7's on full load or two full racks on light load (say 10ma load current). One PU7 will drive two A7's on full load or four on light load.

The specified output of ± 100V at 50mA implies a minimum load resistance, including the feedback resistor in parallel, of 2K. If the load is less than 2K additional series resistance should be added to bring it up to 2K or the voltage swing should be restricted. At approximately - 100ma the overload circuits start to operate and prevent the current rising further. Maximum capacity loading is .01uF at the output.

Connections to the amplifier are shown on the back plate. The amplifier is designed to give considerable flexibility in fitting feedback components. For computer type applications the components are normally remote from the amplifier and connections are made to the socket at the rear. For fixed purpose applications components may be fitted internally on the amplifier printed board provided they are not too large. The position for them is shown in an insert on the circuit diagram. Access to the face of the board is obtained by removing the four screws holding it to the metal plate. It is also possible to connect temporary components by using the monitor points on the front panel. The amplifier is tested for noise, drift, etc. at a gain of 1000 using 1K for Z_i, 1M for Z_f. These values will be found convenient for checking the amplifier.

It will be seen from the circuit diagram that there is a 33pf capacitor C3 between the output and the summing junction. This limits the closed loop bandwidth for high values of Z_f. It can be compensated for by connecting a corresponding capacitor across Z_i having a value chosen to make the ratio of reactances correspond to the ratio of resistances. Thus for Z_f = 1M Z_i = 1K .033uF is required across Z_i.

3. Operating Instructions

The amplifier can be tested initially lying flat on the bench by fitting a socket and connecting up power supplies and feedback components. The input to Z_i should be connected to common and the power supplies arranged so that both lines can be switched on simultaneously.

The front panel carries three indicator lamps. The first two indicate operation of overload protection circuits, the third is a limit lamp which indicates when the amplifier has reached a maximum in either direction. When the unit is initially switched on the limit lamp will light until the amplifier settles down to give zero output.

Two zero controls are provided. RV1 on the front panel is a fine control giving a current offset of ± 4nA which corresponds to ± 50mV at the output at a gain of 1000, with 1K, 1M feedback. RV2 is a coarse control which is accessible from the bottom of the amplifier. This is used to set the output at zero when the fine control is in the centre of its range. A warming up time of a quarter of an hour should be allowed before these zero controls are adjusted. A signal at, say, 1Kc/s can be applied to the input terminals to check that the amplifier is working normally and it can then be fitted in its final position.

4. Circuit Description

The A7 consists of a photoconductive chopper amplifier operating at DC and low frequencies which is bypassed by an AC channel operating at higher frequencies. The combined frequency response gives a maximum gain at DC of 3×10^7 falling at 6db per octave to a flat mid band region extending from 10c/s to 1Kc/s with gain in the region of 10^5. Above 1Kc/s the gain falls in an approximation to the ideal Bode characteristic at about 9db per octave.

The chopper amplifier comprises VT6 to VT13. PR1 and 2 are cadmium selenide cells connected to give combined series-shunt chopper operation. These cells are illuminated alternately by

neons N1 and N2 which are driven by transistors VT14 and 15 at about 300c/s. The demodulator is a transistor VT10 which is driven synchronously with N2. This is followed by filter circuits which remove the chopper ripple. Both the emitter follower VT11 and the integrator, VT12 and VT13, have temperature compensating circuits.

Transistors VT1 to 5 form the high frequency amplifier. The output of both channels is combined at the base of VT16, which together with the level shifting emitter follower VT17, provides the drive signal for the output stage. This is a class B stage consisting of VT18, VT19 and VT20. It will be seen that VT18 drives the output load on negative half cycles with VT19 and 20 cut off by the voltage drop across diodes MR13 and MR15. On positive half cycles the current through VT18 is reduced and VT19 and VT20 provide the drive.

The remaining circuits are concerned with protection against overload, the positive and negative lines being protected separately. Considering first VT22 and VT23 it will be seen that when current through the sensing resistor R64 is low, VT22 is cut off and therefore VT22 is held on via MR18. If the current through R64 exceeds about 100mA then VT22 starts to conduct and completes the circuit through MR19 and VT21, holding down the base of VT19 thus preventing the current rising further. This condition is maintained for about a second during which time C26 charges through R71. If the overload is not removed ILP2 fires causing VT22 to saturate and completely remove the drive to VT19. Complementary circuits including VT24 and VT25 perform corresponding functions if excess current is taken from the negative line. ILP2 and ILP3 are brought out to the front panel to give visual warning of overload.

5. Fault Finding

The amplifier may be serviced by removing the four screws holding the printed board to the metal plate. It will stand on the bench like an open book, power supplies and feedback components being connected by the use of a free socket as in the operating instructions. Standing it upside down allows easy adjustment of the coarse zero control. It is also possible to check that the chopper drive neons are working as the glow is visible through the holes in the base of the chopper block.

Examination of the circuit diagram shows that the amplifier is divided into sections each one of which is required to set itself up to the proper operating DC levels, either by local or overall feedback, before the amplifier as a whole will function correctly. The preliminary test procedure therefore consists of checks of power supply voltages, measurement of DC levels at a few selected points in the circuit with checks to establish that the chopper channel has settled to a null and the amplifier output to zero. The procedure is as follows.

Check that plus and minus 150V are being applied then measure the 10V auxiliary lines with respect to common. (These are available at the lower ends of R49 to R52, the four large resistors nearest the front panel on the heat sink). The tolerance on the 10V lines is ± 10%.

The H.F. amplifier is checked by measuring the voltage at the collector of VT5 which should be 6.5V ± .75V. The voltage at VT9 collector (5V ± 1V) indicates correct functioning of the chopper amplifier. Its output can be checked with an oscilloscope on either side of MR4. This should be a characteristic 300c/s waveform of not more than 1V peak-to-peak. The integrator (VT13 collector) should set up at 5V ± 2V and the driver transistors (VT16c and VT17c) should be at about -40V and -1.5V respectively.

The most likely effect of a fault will be to prevent the amplifier output settling to zero with zero input and the method of locating it is to check DC voltages at the above points, starting from the output and working back through the amplifier looking for an anomaly. Thus if the output is fully positive VT17c should be low, VT16c high (i.e. more negative) VT13c more positive, etc. Suppose for example VT13c was low under these conditions, it would point to a fault in the region of VT16.

Faults in the overload circuits are likely to be indicated by operation of an overload lamp when no overload is present and are located by checking the circuits with respect to the lines. For example VT22 should be normally off with a collector voltage of about -96V with respect to +150 set by MR18. VT23c should be within a volt of +150. Similar reasoning applies to VT24 and VT25.

In case of difficulty, advice or assistance may be obtained by writing or telephoning the manufacturers.

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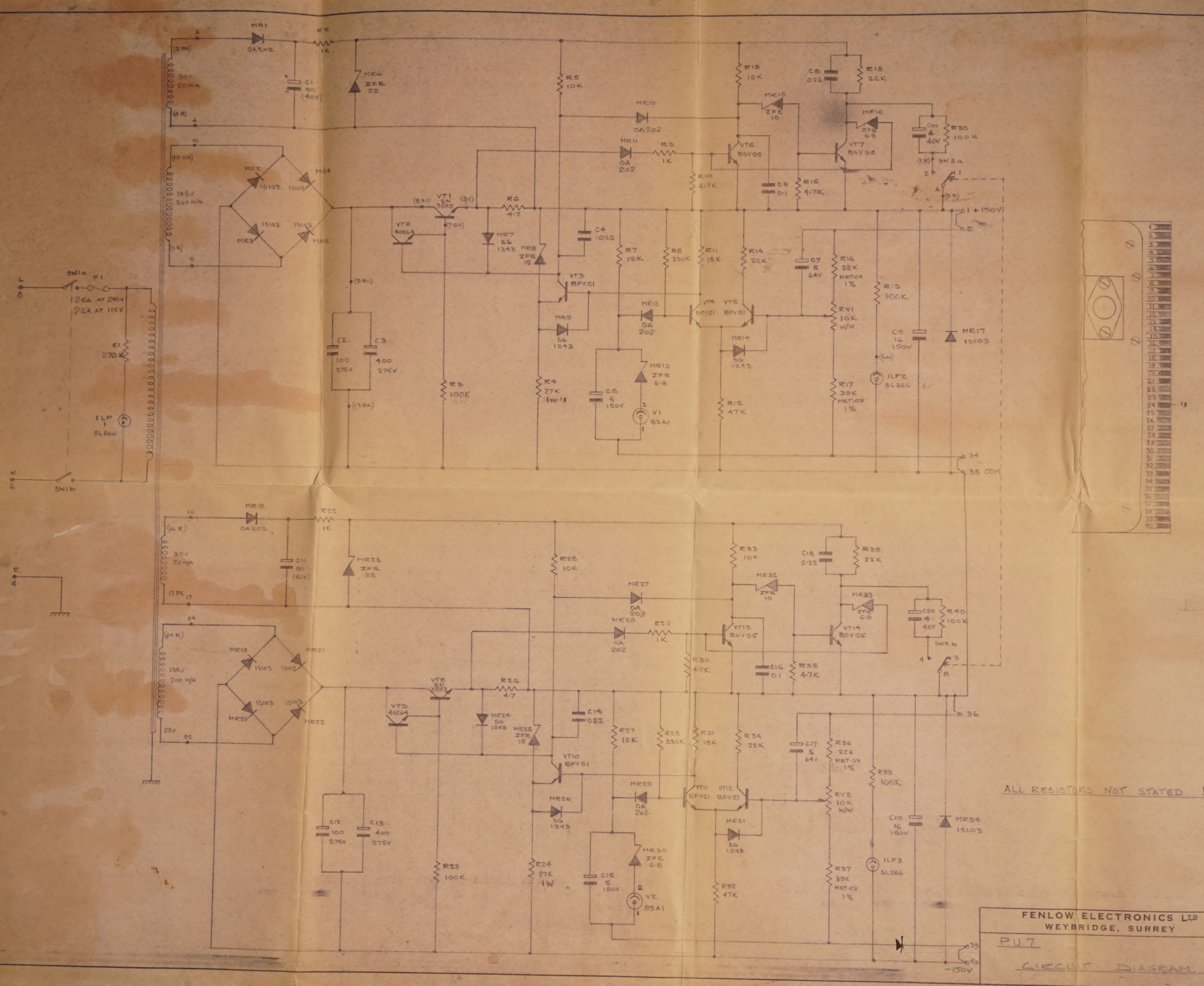

CHANGES
VARIOUS VALUE CHANGES AND PLUG PIN DETAILS ADDED ISSUE 2.
MR 10, 11, 12, 27, 28, 29 WERE SG 1243 1658
2 GR WAS 1A

PART Nº/ASSY. Nº				
MATERIAL :-				
FINISH :-				
UNSTATED TOLERANCES ± 0·015"				
DRG. Nº C11780				

FENLOW ELECTRONICS LTD WEYBRIDGE, SURREY	DATE	DR'N	CH'K'D	ISSUE
	21/9/65	GWT	[illegible]	1
	27/10/65	GWT	EC	2
	13/12/65	JET	JET	3
	2·3·65	JET	JET	4
P.U.7				
CIRCUIT DIAGRAM.				

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